Electronics OEMs benefit from boundary-scan technology

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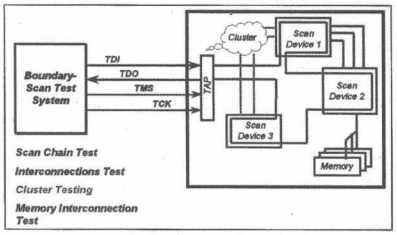
The rapid increase in complexity of electronic devices and pc boards challenges today's manufacturers to find and exploit new methods to accomplish production objectives. The problems of limited physical access, increased production throughput objectives and shorter time-to-market all conspire for a more challenging manufacturing environment.



Multiple functions can be performed at high speed.

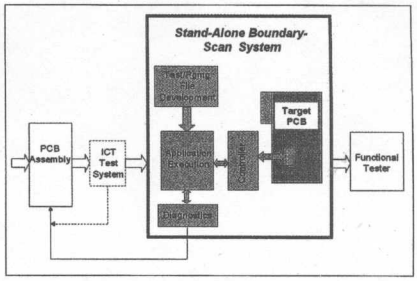
A proven solution to these issues is boundary-scan, a technique gaining increasing acceptance throughout the electronics industry. Boundary-scan is based on the IEEE 1149.1 specification, which was developed more than 10 years ago by a consortium of electronics manufacturers.

The work grew out of concern that packaging trends would soon advance to the point where physical access would become impossible, obstructing effective testing of printed circuit boards. The Joint Test Action Group's (JTAG) foresight was indeed accurate.

Initially, boundary-scan was intended to support board and chip level test access. In exchange for the addition of gates and shift registers to ICs, boundary-scan restores the electrical access that board manufacturers were in danger of losing. In place of parallel access using a large number of test points, boundary-scan provides access over a serial port requiring only a small number of contacts.

Going beyond the initial plan, boundary-scan is also being used very effectively for system level testing and for in-system programming of CPLDs and flash memory devices. Each of these applications provides great value to OEMs.

Traditional board testing can be grouped into two general techniques:



Boundary-scan readily integrates with other test strategies.

in-circuit and functional. Although both methods are intended to find faults in products before shipment, they differ substantially in their approach to the problem.

In-circuit testing (ICT) typically relies on electrical access to test points on the board by means of a custom fixture consisting of a large number of electrical probes. The test system drives the circuit and senses its responses via the test points based on a programmed sequence of test vectors.

The creation of tests for ICT is usually performed with automatic pattern generators based on libraries of component characteristics. The test designer must take into account a detailed understanding of the target board, in order to create an effective test and to avoid imposing undesirable or possibly damaging vectors on the board.

ICT has been used very effectively for many years, but present-day board densities have pushed the method to its limits. The number of test points can exceed 4,000, accompanied by great expense and fragility of the test fixture. Going beyond a simple number of test points, SMT and chip-size packages such as BGA severely limit the possibility of electrical access. For these reasons, test coverage, the measure of possible structural faults that can be detected, continues to decrease and may jeopardize meeting corporate quality objectives. On the positive side, faults that can be detected via ICT are usually diagnosed precisely, so repair is swift.

The objective of functional testing is to verify that an assembled board performs as its designer intends, usually by stimulating it through its board-edge connectors or other access points. Typically, the board is activated close to its normal mode of operation and the results are compared to the expected function.

Unfortunately, there are no automatic test generators for functional testing, so test design is labor-intensive and, when an error is detected, troubleshooting is often difficult and slow because a large number of different faults can cause the same failure. Most production facilities have a bonepile attesting to the difficulty of fault diagnosis.

OEMs have often turned to functional testing to find manufacturing faults if they find the expense of ICT prohibitive, or if they need to verify the functionality of the board after ICT.

The traditional means of programming ICs is to place them in a device programmer prior to board assembly, perform the desired programming and install them in the pcbs later in the manufacturing process. For many years, this method worked fine, but as devices have become smaller and as manufacturers have worked to reduce process costs and accelerate their time-to-market, there has been increasing interest in on-board programming after pcb assembly.

Initial attempts to perform on-board programming use the ICT by means of test point contact with the programmable device's address, data and control pins. This method, however, is impeded by the same access problems that hinder testing; as boards become denser and devices smaller, the lack of physical access prevents successful programming. Fortunately, as there is a common denominator to test and programming problems, there is also a common solution.

Boundary-scan accesses the board by means of scan registers within the ICs. The impact of SMT and chip-size packages on electrical access are completely overcome, giving the test or programming system the ability to drive or sense

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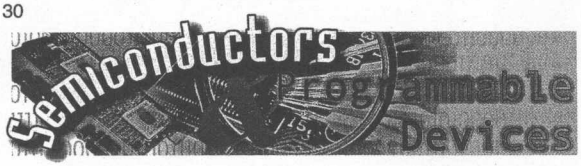


Boundary scan

continued from page 28

every pin on every scannable device.

Among the strengths of boundary-scan are:

- Automatic test generation of the scannable portion of the board.
- Back-drive and other unintended circuit interactions can be completely avoided.
- Pin-point fault diagnosis is possible for the portions of the circuit that employ boundary-scan.
- Bed-of-nails fixturing is greatly simplified or eliminated.
- Programming is done after assembly, reducing the handling of devices and simplifying the inventory management.

Balancing the strengths, there are these considerations:

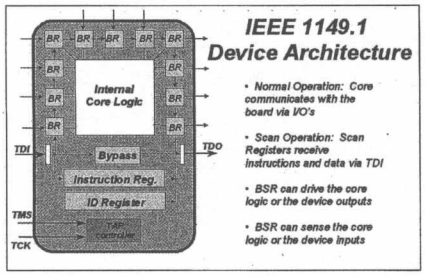
- Analog circuits, at present, are not testable using boundary-scan.
- Boards must be designed for testability and programmability ahead of time, using boundary-scan techniques, selection of appropriate ICs and provision of scan chain access.
- Clusters of devices without boundary-scan may be difficult to test and/or diagnose.

In many cases, a practical test strategy would be to use a combination of boundary-scan plus ICT or functional test. If properly partitioned between methods, the designer can realize benefits of both approaches and avoid the drawbacks.

In one example, based on a real-world application, a complex circuit board with more than 4000 parallel test points contains both analog and digital circuits. The designer decides to use boundary-scan to test the digital portion of the board and to continue using ICT for the analog portion as well as for clusters that are not accessible from the scan chain.

The combination results in a significant increase in fault coverage and a sharp reduction in the cost of the ICT test fixture. Also, the mixed solution avoids further investment in costly ICTs and reduces expenses for fixtures.

Boundary-scan tests are generated automatically, and faults are diagnosed with pin-level accuracy. Cost of the boundary-scan system is typically a fraction of the ICT system. ***For more information on boundary-scan test products from JTAG Technologies, circle 586 on Reader Service Card or at*** www.ept.ca



IEEE 1149.1 standard makes boundary-scan implementation possible.

CEL lab installs noise tester

California Eastern Laboratories (CEL), Santa Clara CA, and ATN Microwave, North Billerica MA, have jointly installed, at CEL's engineering support lab, an automated noise parameter test system developed by Microvue Inc., which was acquired by ATN late 1998. The system makes measurement of extremely low-noise devices easier and more precise, and simplifies the characterization of high-gain parts that are hard to measure.

The system consists of two Wavevue software modules. One measures S-parameters and dc characteristics and the other noise. The software and technical improvements will form the basis for a new NP5C noise parameter system from ATN.

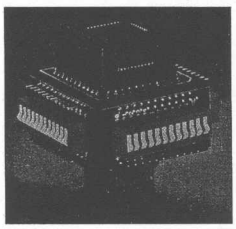
The system is able to generate and process data in hours that used to take weeks, according to the manager of CEL's engineering lab Abby O'Connell. Data are delivered assembled and plotted for immediate use by CEL customers and can be directly downloaded to CAD programs.

CEL celebrates 40th anniversary

California Eastern Laboratories (CEL), Santa Clara CA, one of Silicon Valley's original technology companies, celebrated its 40th anniversary on August. Among the first American companies to introduce Japanese technology to the North American market, today it represents NEC's RF, wireless and optoelectronic semiconductor products exclusively and operates a Design Center with NEC at its Santa Clara headquarters.

With sales of over US $89-million last year, CEL is one of the 100 largest private companies in California and the largest employee-owned company in Silicon Valley. In a recent survey by Electronic Buyers News, it was ranked as the 23rd largest electronics distributor in the U.S. and 11th largest semiconductor distributor. The company has field sales offices throughout North America as well as a network of independent distributors.

Modules allow IC pin isolation



Winslow pin isolation modules enable the segregation of individual integrated circuit pins. Modules plug into a motherboard IC socket or, with "clip over" option, attach directly to board mounted ICs. They come in various package styles, including PGA, PLCC and dual-in-line, and can be supplied with standard ZIP sockets.

Dual-in-line switches can activate or deactivate any IC pins, induce faults under controlled conditions or disable unwanted interrupt and resets when emulating. Custom packages are available for use with QFPs.

S-P INTERNATIONAL

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Gullwing emulator feet pass signals to µGA pins

SF-QFE128SD-G-01 gullwing 0.4mm pitch leaded surface mount emulator feet for fine pitch ICs with small packaging make signals available at µGA (micro grid array) pins on top of the feet. µGA sockets connect daughter boards, upgrade cards and other circuitry to the surface mount lands on a target pcb.

Compliant leads solder easily to a target board land pattern intended for a gull-wing package using simple hand soldering procedures.

IRONWOOD ELECTRONICS

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